

TLE7182EM

H-Bridge and Dual Half Bridge Driver IC

Automotive Power



Never stop thinking

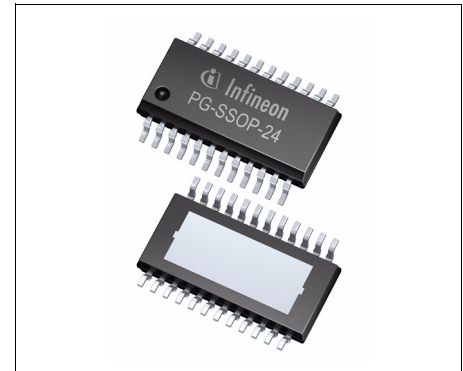
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H-Bridge and Dual Half Bridge Driver IC

1 Overview
Features

- Drives 4 N-Channel Power MOSFETs
- Separate control input for each MOSFET
- Unlimited D.C. switch on time of Low and Highside MOSFETs
- 0 ... 95% at 20kHz & 100% Duty cycle of High Side MOSFETs
- 0 ... 100 % Duty cycle of Low Side MOSFETs
- Additional output to drive a reverse polarity protection N-MOSFET
- Current sense OPAMP
- Low quiescent current mode
- Internal shoot through protection and minimum internal dead time option
- 1 bit diagnosis / ERR
- Over current warning based on current sense OPAMP with fixed warning level
- Analog adjustable Short Circuit Protection levels via SCDL pin with open pin detection and SCD deactivation
- Over temperature warning
- Over voltage warning
- Under voltage warning and shutdown
- Green Product (RoHS compliant)
- AEC Qualified


PG-SSOP-24
Description

The TLE7182EM is a H-bridge driver IC dedicated to control 4 N-channel MOSFETs typically forming the converter for a high current DC motor drives in the automotive sector. It incorporates several protection features such as over current and short circuit detection as well as under-, over voltage and over temperature diagnosis.

The TLE7182EM perfectly fits for driving 2 valves or solenoids too.

Typical applications are fans, pumps and electric power steering. The TLE7182EM is designed for a 12V power net.

Table 1 Product Summary

| | | |
|-----------------------------------------|------------|-----------------|
| Specified operating voltage | V_{SOP} | 7.0 V ... 34 V |
| Junction temperature | T_j | -40 °C .. 150°C |
| Maximum output source resistance | R_{Sou} | 13.5 Ω |
| Maximum output sink resistance | R_{Sink} | 9 Ω |
| maximum quiescent current ¹⁾ | I_{QVS} | 8 μ A |

1) typical value at $T_j=25^\circ\text{C}$

| Type | Package | Marking |
|-----------|------------|-----------|
| TLE7182EM | PG-SSOP-24 | TLE7182EM |

2 Block Diagram

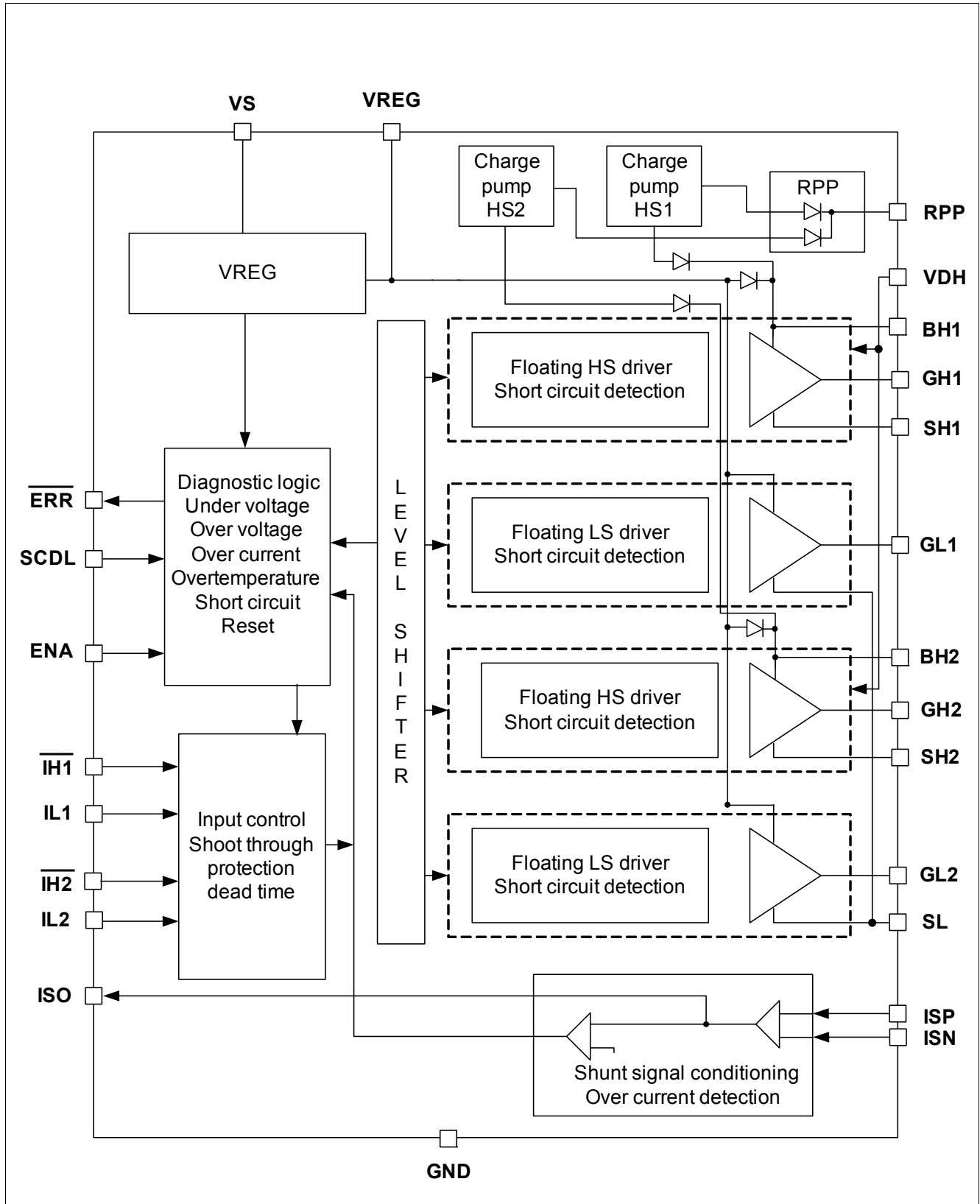


Figure 1 Block diagram TLE7182EM

3 Pin Configuration

3.1 Pin Assignment

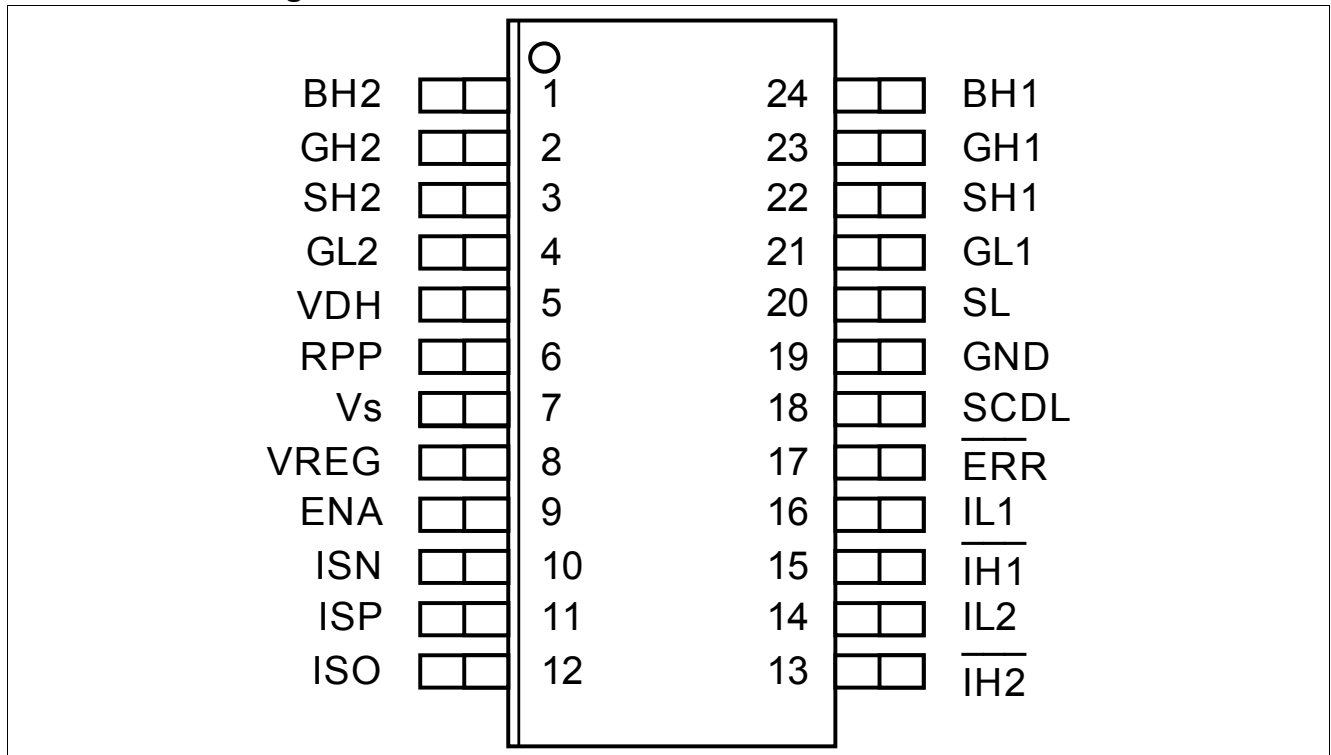


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

| # of Pins | Symbol | Function |
|-----------|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | BH2 | Pin for + terminal of the bootstrap capacitor of phase 2 |
| 2 | GH2 | Output pin for gate of high side MOSFET 2 |
| 3 | SH2 | Pin for source connection of high side MOSFET 2 |
| 4 | GL2 | Output pin for gate of low side MOSFET 2 |
| 5 | VDH | Voltage input common drain high side for short circuit detection |
| 6 | RPP | charge pump output for reverse polarity protection of the motor bridge |
| 7 | VS | Pin for supply voltage |
| 8 | VREG | Output of supply for driver output stage - connect to a capacitor |
| 9 | ENA | Input pin for reset of $\overline{\text{ERR}}$ registers, active switch off of external MOSFETs and low quiescent current mode, set HIGH to enable operation |
| 10 | ISN | Input for OPAMP + terminal |
| 11 | ISP | Input for OPAMP - terminal |
| 12 | ISO | Output of OPAMP |
| 13 | $\overline{\text{IH2}}$ | Input for high side switch 2 (active low) |
| 14 | $\overline{\text{IL2}}$ | Input for low side switch 2 (active high) |
| 15 | $\overline{\text{IH1}}$ | Input for high side switch 1 (active low) |
| 16 | $\overline{\text{IL1}}$ | Input for low side switch 1 (active high) |

Pin Configuration

| # of Pins | Symbol | Function |
|-----------|-------------------------|--------------------------------------------------------------------------------|
| 17 | $\overline{\text{ERR}}$ | Push pull output stage |
| 18 | SCDL | Input pin for adjustable Short Circuit Detection function and SCD deactivation |
| 19 | GND | Ground pin |
| 20 | SL | Pin for common source of lowside MOSFETs |
| 21 | GL1 | Output pin for gate of low side MOSFET 1 |
| 22 | SH1 | Pin for source connection of high side MOSFET 1 |
| 23 | GH1 | Output pin for gate of high side MOSFET 1 |
| 24 | BH1 | Pin for + terminal of the bootstrap capacitor of phase 1 |
| Tab | Tab | should be connected to GND |

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings ¹⁾

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|---------------------------|-------------------------------------------------|-------------------|--------------|------|------|------------------------------------------------------------------|
| | | | Min. | Max. | | |
| Voltages | | | | | | |
| 4.1.1 | Supply voltage at VS | V _{VS} | -0.3 | 45 | V | – |
| 4.1.2 | Supply voltage at VS | V _{VSRP} | -4.0 | 45 | V | R _{VS} ≥ 10Ω |
| 4.1.3 | Voltage range at VDH | V _{VDH} | -0.3 | 55 | V | – |
| 4.1.4 | Voltage range at RPP | V _{RPP} | -0.3 | 55 | V | – |
| 4.1.5 | maximum current at RPP | I _{RPP} | -25 | 25 | mA | – |
| 4.1.6 | Voltage range at ENA | V _{ENA} | -0.3 | 45 | V | – |
| 4.1.7 | Voltage range at SCDL | V _{SCDL} | -0.3 | 6 | V | – |
| 4.1.8 | Voltage range at IH1, IL1, IH2, IL2 | V _{DPI} | -0.3 | 6 | V | – |
| 4.1.9 | Voltage range at ERR, ISO | V _{DPO} | -0.3 | 6 | V | – |
| 4.1.10 | Voltage range at ISP, ISN | V _{OPI} | -5.0 | 5.0 | V | – |
| 4.1.11 | Voltage range at VREG | V _{VREG} | -0.3 | 15 | V | – |
| 4.1.12 | Voltage range at BHx | V _{BH} | -0.3 | 55 | V | – |
| 4.1.13 | Voltage range at GHx | V _{GH} | -0.3 | 55 | V | – |
| 4.1.14 | Voltage range at GHx | V _{GHP} | -7.0 | 55 | V | t _p < 1μs; f = 50kHz |
| 4.1.15 | Voltage range at SHx | V _{SH} | -2.0 | 45 | V | – |
| 4.1.16 | Voltage range at SHx | V _{SHP} | -7.0 | 45 | V | t _p < 1μs; f = 50kHz |
| 4.1.17 | Voltage range at GLx | V _{GL} | -0.3 | 18 | V | – |
| 4.1.18 | Voltage range at GLx | V _{GLP} | -7.0 | 18 | V | t _p < 0.5μs; f = 50kHz |
| 4.1.19 | Voltage range at SL | V _{SL} | -1.0 | 5.0 | V | – |
| 4.1.20 | Voltage range at SL | V _{SLP} | -7.0 | 5.0 | V | t _p < 0.5μs; f = 50kHz; C _{BS} ≥ 330nF |
| 4.1.21 | Voltage difference Gxx-Sxx | V _{GS} | -0.3 | 15 | V | – |
| 4.1.22 | Voltage difference BHx-SHx | V _{BS} | -0.3 | 15 | V | – |
| Temperatures | | | | | | |
| 4.1.23 | Junction temperature | T _j | -40 | 150 | °C | – |
| 4.1.24 | Storage temperature | T _{stg} | -55 | 150 | °C | – |
| 4.1.25 | Lead soldering temperature (1/16" from body) | T _{sol} | – | 260 | °C | – |
| 4.1.26 | Peak reflow soldering temperature ²⁾ | T _{ref} | – | 260 | °C | – |
| Power Dissipation | | | | | | |
| 4.1.27 | Power Dissipation (DC) | P _{tot} | – | 2 | W | – |
| ESD Susceptibility | | | | | | |
| 4.1.28 | ESD Resistivity ³⁾ | V _{ESD} | – | 2 | kV | – |

Absolute Maximum Ratings (cont'd)¹⁾
 $40\text{ °C} \leq T_j \leq 150\text{ °C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|--------|-----------|------------------|--------------|------|------|------------|
| | | | Min. | Max. | | |
| 4.1.29 | CDM | V_{CDM} | – | 1 | kV | |

- 1) Not subject to production test, specified by design.
- 2) Reflow profile IPC/JEDEC J-STD-020C
- 3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

| Pos. | Parameter | Symbol | Limit Values | | Unit | Conditions |
|--------|-----------------------------------------------------|--------------------|--------------|----------|---------------|--------------------------------------------------------------------------------------------------------|
| | | | Min. | Max. | | |
| 4.2.1 | Specified supply voltage range | V_{VS1} | 7.0 | 34 | V | – |
| 4.2.2 | supply voltage range ¹⁾ | V_{VS2} | 5.5 | 45 | V | $V_{\text{VS}} < 7\text{V}$ reduced functionality |
| 4.2.3 | Quiescent current at VS | I_{QVS1} | – | 8 | μA | $V_{\text{VS}}, V_{\text{VDH}} = 12\text{V}$; ENA=Low; $T_j = 25\text{ °C}$ |
| 4.2.4 | Quiescent current at VS | I_{QVS2} | – | 10 | μA | $V_{\text{VS}}, V_{\text{VDH}} < 15\text{V}$; ENA=Low; $T_j \leq 85\text{ °C}$ |
| 4.2.5 | Quiescent current at VDH | I_{QVDH1} | – | 8 | μA | $V_{\text{VS}}, V_{\text{VDH}} = 12\text{V}$; ENA=Low; $T_j = 25\text{ °C}$ |
| 4.2.6 | Quiescent current at VDH | I_{QVDH2} | – | 10 | μA | $V_{\text{VS}}, V_{\text{VDH}} < 15\text{V}$; ENA=Low; $T_j \leq 85\text{ °C}$ |
| 4.2.7 | Supply current at Vs (device enabled) ²⁾ | $I_{\text{Vs(1)}}$ | – | 22 | mA | no switching |
| 4.2.8 | Supply current at Vs (device enabled) | $I_{\text{Vs(2)}}$ | – | 45 | mA | $4 \times Q_{\text{GS}} \times f_{\text{PWM}} \leq 20\text{mA}$; $V_{\text{VS}} = 7.0..34\text{V}$ |
| 4.2.9 | D.C. switch on time of output stages | D_{DC} | – | ∞ | s | – |
| 4.2.10 | Duty cycle Highside output stage ³⁾ | D_{HS} | 0 | 95 | % | $f_{\text{PWM}} = 20\text{kHz}$; continuous operation; $C_{\text{BS}} \geq 330\text{nF}$ |
| 4.2.11 | Duty cycle Lowside output stage | D_{LS} | 0 | 100 | % | – |

- 1) operation above 34V limited by max. allowed power dissipation and max. ratings
- 2) Current can be higher, if driver output stages are unpowered
- 3) max. limit of D.C. will increase, if f_{PWM} or external gate charge of the MOSFETs is reduced

The PWM frequency is limited by thermal constraints and the maximum duty cycle (minimum charging time of bootstrap capacitor).

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|-------|-----------------------------------|------------|--------------|------|------|------|---------------|
| | | | Min. | Typ. | Max. | | |
| 4.3.1 | Junction to Case ¹⁾ | R_{thJC} | – | – | 5 | K/W | – |
| 4.3.2 | Junction to Ambient ¹⁾ | R_{thJA} | – | 35 | – | K/W | ²⁾ |

1) Not subject to production test, specified by design.

2) **Exposed Heatslug Package use this sentence:** Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 μ m Cu, 2 x 35 μ m Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.4 Default State of Inputs

Table 2 Default State of Inputs (if left open)

| Characteristic | State | Remark |
|-----------------------|-------|------------------------------------------------|
| Default state of IHx | High | High side MOSFETs off |
| Default state of ILx | Low | Low side MOSFETs off |
| Default state of ENA | Low | Output stages disabled device in sleep mode |
| Default state of SCDL | OPEN | Short circuit detection deactivation & warning |

5 Description and Electrical Characteristics

5.1 MOSFET Driver

5.1.1 Driving MOSFET Output Stages

The TLE7182EM incorporates 2 high side and low side output stages for 4 external MOSFETs.

Unlike other H-Bridge drivers the TLE7182EM offers 4 independent control inputs to control the MOSFETs individually. However, the control inputs for the Highs Side MOSFETs I_{Hx} are inverted. Hence, the control inputs for High Side I_{Hx} and Low Side MOSFETs I_{Lx} of the same half bridge can be tight together to control one half bridge by one control signal. To avoid shoot through currents within the half bridges, a minimum dead time is provided by the TLE7182EM. Minimum dead time is only generated, if the short circuit detection is activated.

If the TLE7182EM drives a load in between the high side MOSFET and the low side MOSFET or the driver is used to drive 4 low side MOSFETs, the short circuit detection and the minimum dead time has to be deactivated by pulling the SCDL pin to 5V.

For more details about the dead time please see [Chapter 5.1.3](#).

[Table 3](#) and [Table 4](#) show the differed states of the output stages subject to the input conditions for activated and deactivated shout through protection.

Table 3 Truth table (shoot through active)

| ENA | IL1 | I $\overline{H1}$ | IL2 | I $\overline{H2}$ | Lowside switch1 | Highside switch1 | Lowside switch2 | Highside switch2 |
|-----|-----|-------------------|-----|-------------------|-----------------|------------------|-----------------|------------------|
| 0 | x | x | x | x | OFF | OFF | OFF | OFF |
| 1 | 0 | 1 | 0 | 1 | OFF | OFF | OFF | OFF |
| 1 | 0 | 0 | 0 | 0 | OFF | ON | OFF | ON |
| 1 | 1 | 1 | 0 | 0 | ON | OFF | OFF | ON |
| 1 | 0 | 0 | 1 | 1 | OFF | ON | ON | OFF |
| 1 | 1 | 1 | 1 | 1 | ON | OFF | ON | OFF |

Table 4 Truth table (shoot through inactive)

| ENA | IL1 | I $\overline{H1}$ | IL2 | I $\overline{H2}$ | Lowside switch1 | Highside switch1 | Lowside switch2 | Highside switch2 |
|-----|-----|-------------------|-----|-------------------|-----------------|------------------|-----------------|------------------|
| 0 | x | x | x | x | OFF | OFF | OFF | OFF |
| 1 | 0 | 1 | 0 | 1 | OFF | OFF | OFF | OFF |
| 1 | 0 | 0 | 0 | 1 | OFF | ON | OFF | OFF |
| 1 | 1 | 0 | 0 | 1 | ON | ON | OFF | OFF |
| 1 | 0 | 1 | 0 | 0 | OFF | OFF | OFF | ON |
| 1 | 0 | 1 | 1 | 0 | OFF | OFF | ON | ON |

5.1.2 MOSFET Output Stages

The six push-pull MOSFET driver stages of the TLE7182EM are realized as separate floating blocks. This means that the output stage is follows the individual MOSFET source voltages and so ensuring stable MOSFET driving even in harsh electrical environment.

All 4 output stages have the same output power and thanks to the used bootstrap principle they can be switched all up to high frequencies.

Each output stage has its own short circuit detection block. For more details about short circuit detection see [Chapter 5.2.1](#).

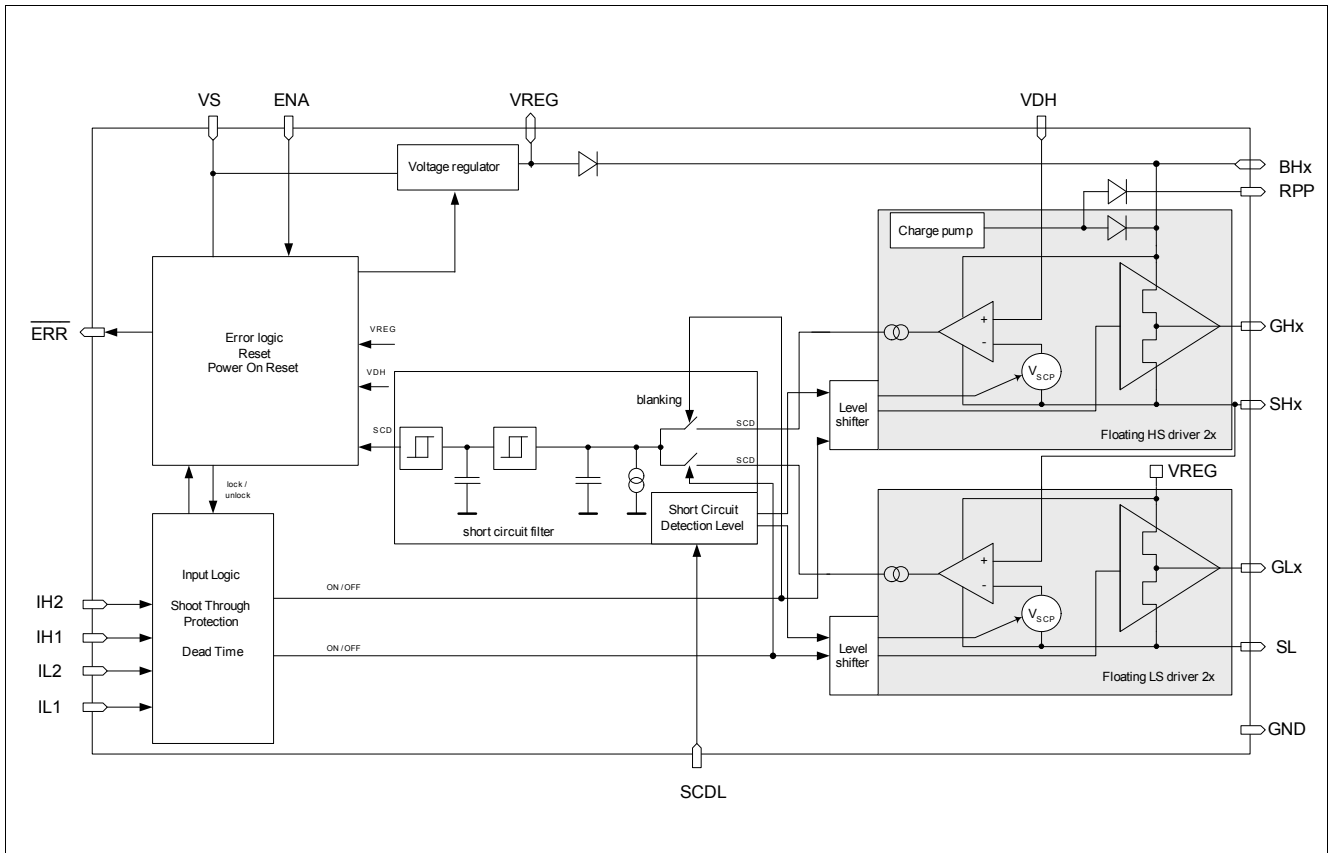


Figure 3 Block Diagram of Driver Stages including Short Circuit Detection

5.1.3 Dead Time and Shoot Through Protection

In bridge applications it has to be assured that the external high side and low side MOSFETs are not “on” at the same time, connecting directly the battery voltage to GND.

In TLE7182EM a minimum dead time applied. It is fixed internally and can not be programmed.

If an exact dead time of the bridge is needed, the use of the μC PWM generation unit is recommended.

In addition to this dead time, the TLE7182EM provides a locking mechanism, avoiding that both external MOSFETs of one half bridge can be switched on at the same time. This functionality is called shoot through protection. If the command to switch on both high and low side switches in the same half bridge is given at the input pins, the command will be ignored. The outputs will stay in the situation like before the conflicting input.

The Shoot through protection and the dead time of the TLE7182EM will be deactivated, if a voltage of 5V is applied at pin SCDL. The deactivation of the shoot through protection is necessary to drive valves or solenoids which are designed in between the Lowside and Highside MOSFET of one half bridge or 4 separate low side MOSFETs.

For more detailed information how to drive valves or solenoid in between one half bridge please see [Figure 7](#).

5.1.4 Bootstrap Principle

The TLE7182EM provides a bootstrap based supply for its high side output stages.

The bootstrap capacitors are charged by switching on the external low side MOSFETs, connecting the bootstrap capacitor to GND. Under this condition the bootstrap capacitor will be charged from the VREG capacitor via the integrated bootstrap diode. If the low side MOSFET is switched off and the high side MOSFET is switched on, the bootstrap capacitor will float together with the SHx voltage to the supply voltage of the bridge. Under this condition the supply current of the high side output stage will discharge the bootstrap capacitor. This current is specified.

The size of the capacitor together with this current will determine how long the high side MOSFET can be kept on without recharging the bootstrap capacitor.

5.1.5 100% D.C. charge pumps

100% D.C. charge pumps are implemented for each high side output stage. Therefore the high side output stages can be switch on for an unlimited time. These integrated charge pumps can handle leakage currents which will be caused by external MOSFETs and the TLE7182EM itself. They are not strong enough to drive a 99% duty cycle for a longer time. the charge pumps are running when the driver is not in sleep mode and assure that the bootstrap capacitors are charged as long as the user does not apply critical duty cycle for a longer time.

5.1.6 Reverse polarity protection of motor bridge

The TLE7182EM provides an additional RPP pin to protect motor bridge for reverse polarity. This RPP pin can drive an additional external N-channel power MOSFET designed in between battery and the motor bridge. The RPP pin is internally supplied by the two integrated 100% D.C. charge pumps. They are especially designed to handle additional current which is needed to drive a the gate charge of the reverse polarity MOSFET. The guarantied output current of the charge pumps is specified.

5.1.7 Sleep mode

If ENA pin is set to low, the ERR flag will be set to low and the output stages will be switched off.

After ENA pin is kept low for t_{LOM} the sleep mode of the Driver IC will be activated.

In Sleep mode the complete chip is deactivated. This means the internal supply structure of the TLE7182EM will be switched off. This mode is designed for lowest current consumption from the power net of the car. The passive clamping is active. For details see the description of passive clamping, see [Chapter 5.2.8](#).

The TLE7182EM will wake up, if ENA is set to high. The ENA pin is 45V compatible, so ENA can be directly be connected to the ignition key signal KL15.

5.1.8 Electrical Characteristics

Electrical Characteristics MOSFET Drivers

$V_S = 7.0$ to $34V$, $T_j = -40$ to $+150^\circ C$ all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|-----------------------|--------------------------------------|-------------|--------------|------|------|------------|----------------------------------|
| | | | Min. | Typ. | Max. | | |
| Control inputs | | | | | | | |
| 5.1.1 | Low level input voltage of Ixx | V_{I_LL} | – | – | 1.0 | V | – |
| 5.1.2 | High level input voltage of Ixx | V_{I_HL} | 2.0 | – | – | V | – |
| 5.1.3 | Input hysteresis of Ixx | d_{VI} | 100 | 200 | – | mV | – |
| 5.1.4 | ILx pull-down resistor to GND | R_{IL} | 320 | 540 | 770 | k Ω | $V_{VS}=0V$ and $VDH=0V$ or open |
| 5.1.5 | ILx pull-down resistor to GND | R_{IL} | 19 | 32 | 50 | k Ω | V_{VS} or $VDH >5.0V$ |
| 5.1.6 | IHx pull-up resistor to internal VDD | R_{IH} | 30 | – | 80 | k Ω | – |
| 5.1.7 | Low level input voltage of ENA | V_{E_LL} | – | – | 0.75 | V | – |
| 5.1.8 | High level input voltage of ENA | V_{E_HL} | 2.1 | – | – | V | – |
| 5.1.9 | Input hysteresis of ENA | d_{VE} | 50 | 200 | – | mV | – |
| 5.1.10 | ENA pull-down resistor to GND | R_{IL} | 70 | 125 | 200 | k Ω | – |

Electrical Characteristics MOSFET Drivers

$V_S = 7.0$ to $34V$, $T_j = -40$ to $+150^\circ C$ all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|-----------------------------|-------------------------------------------------------|------------|---------------------|----------------|------|----------|-----------------------------------------------------------------------------------------------------------|
| | | | Min. | Typ. | Max. | | |
| MOSFET driver output | | | | | | | |
| 5.1.11 | Output source resistance | R_{Sou} | 2 | – | 13.5 | Ω | $I_{Load} = -20mA$ |
| 5.1.12 | Output sink resistance | R_{Sink} | 2 | – | 9.0 | Ω | $I_{Load} = 20mA$ |
| 5.1.13 | High level output voltage Gxx vs. Sxx | V_{Gxx1} | – | 11 | 15 | V | $13.5V \leq V_{VS} \leq 34V$; $I_{Load} = 0mA$ |
| 5.1.14 | High level output voltage Gxx vs. Sxx | V_{Gxx2} | – | 11 | 13.5 | V | $13.5V \leq V_{VS} \leq 34V$; $C_{Load} = 20nF$; D.C. = 50%; $f_{PWM} = 20kHz$ |
| 5.1.15 | High level output voltage GHx vs. SHx ¹⁾ | V_{GHx3} | – | $V_{VS} - 1.5$ | – | V | $7.0V < V_{VS} < 13.5V$; $C_{Load} = 20nF$; D.C. = 50%; $f_{PWM} = 20kHz$ |
| 5.1.16 | High level output voltage GLx vs. GND ¹⁾ | V_{GLx3} | – | $V_{VS} - 0.5$ | – | V | $7.0V < V_{VS} < 13.5V$; $C_{Load} = 20nF$; $f_{PWM} = 20kHz$ & D.C. = 50%; or D.C. = 100% |
| 5.1.17 | High level output voltage GHx vs. SHx ¹⁾²⁾ | V_{GHx4} | 5.0 $+V_{diode}$ | – | – | V | $V_{VS} = 7.0V$; $C_{Load} = 20nF$; D.C. = 95%; $f_{PWM} = 20kHz$; passive freewheeling |
| 5.1.18 | High level output voltage GHx vs. SHx ¹⁾ | V_{GHx5} | 5.0 | – | – | V | $V_{VS} = 7.0V$; $C_{Load} = 20nF$; D.C. = 95%; $f_{PWM} = 20kHz$ |
| 5.1.19 | High level output voltage GLx vs. SLx ¹⁾ | V_{GLx5} | 6.0 | – | – | V | $V_{VS} = 7.0V$; $C_{Load} = 20nF$; D.C. = 95%; $f_{PWM} = 20kHz$ |
| 5.1.20 | High level output voltage GHx vs. SHx ¹⁾ | V_{GHx5} | 10 | – | – | V | $7.0V \leq V_{VS} \leq 13.5V$; $C_{Load} = 20nF$; D.C. = 100% |
| 5.1.21 | High level output voltage GLx vs. SLx ¹⁾ | V_{GLx5} | 6.5 | – | – | V | $V_{VS} = 7.0V$; $C_{Load} = 20nF$; D.C. = 100% |
| 5.1.22 | Rise time | t_{rise} | – | 250 | – | ns | $C_{Load} = 11nF$; |
| 5.1.23 | Fall time | t_{fall} | – | 200 | – | ns | $R_{Load} = 1\Omega$; $V_{VS} = 7V$; 20-80% |

Electrical Characteristics MOSFET Drivers

$V_S = 7.0$ to $34V$, $T_j = -40$ to $+150^\circ C$ all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|--------|---------------------------------------------------------------|-------------|--------------|------|------|------------|--------------------------------------------------------------------------------------------------|
| | | | Min. | Typ. | Max. | | |
| 5.1.24 | High level output voltage (in passive clamping) ¹⁾ | V_{GxxUV} | – | – | 1.2 | V | Sleep mode or VS_UVLO |
| 5.1.25 | Pull-down resistor at BHx to GND | R_{BHUVx} | – | – | 85 | k Ω | Sleep mode or VS_UVLO |
| 5.1.26 | Pull-down resistor at VREG to GND | R_{VRUV} | – | – | 30 | k Ω | Sleep mode or VS_UVLO |
| 5.1.27 | Bias current into BHx | I_{BHx} | – | – | 150 | μA | $V_{CBS} > 5V$; no switching |
| 5.1.28 | Bias current out of SHx | I_{SHx} | – | 40 | – | μA | $V_{SHx} = V_{SL}$; ENA=HIGH; affected highside output stage static on; $V_{CBS} > 5V$ |
| 5.1.29 | Bias current out of SL | I_{SL} | – | – | 1.4 | mA | $0 \leq V_{SHx} \leq V_{VS} + 1V$; ENA=HIGH; no switching; $V_{CBS} > 5V$ |

Dead time & input propagation delay times

| | | | | | | | |
|--------|----------------------------------------------------------------------------|---------------|------|------|-----|---------|---------------------------------------------|
| 5.1.30 | Min. internal dead time | t_{DT_MIN} | 0.08 | 0.11 | 0.2 | μs | – |
| 5.1.31 | Dead time deviation between channels | d_{tDT2} | -15 | – | 15 | % | – |
| 5.1.32 | Dead time deviation between channels LSoft -> HS on | d_{tDT2} | -12 | – | 12 | % | – |
| 5.1.33 | Dead time deviation between channels HSoft -> LS on | d_{tDT2} | -12 | – | 12 | % | – |
| 5.1.34 | Input propagation time (low on) | $t_{P(ILN)}$ | 0 | 100 | 200 | ns | $C_{Load} = 10nF$; $R_{Load} = 1\Omega$ |
| 5.1.35 | Input propagation time (low off) | $t_{P(ILF)}$ | 0 | 100 | 200 | ns | |
| 5.1.36 | Input propagation time (high on) | $t_{P(IHN)}$ | 0 | 100 | 200 | ns | |
| 5.1.37 | Input propagation time (high off) | $t_{P(IHF)}$ | 0 | 100 | 200 | ns | |
| 5.1.38 | Absolute input propagation time difference between above propagation times | $t_{P(diff)}$ | – | 50 | 100 | ns | |

VREG

| | | | | | | | |
|--------|----------------------------------|---------------|-----|------|-----|----|-------------------------------------------------------------|
| 5.1.39 | VREG output voltage | V_{VREG} | 11 | 12.5 | 14 | V | $V_{VS} \geq 13.5V$; $I_{Load} = -35mA$ |
| 5.1.40 | VREG over current limitation | $I_{VREGOCL}$ | 100 | – | 500 | mA | – ³⁾ |
| 5.1.41 | Voltage drop between Vs and VREG | V_{VsVREG} | – | – | 0.5 | V | $V_{VS} \geq 7V$; $I_{Load} = -35mA$; Ron operation |

Electrical Characteristics MOSFET Drivers

$V_S = 7.0$ to $34V$, $T_j = -40$ to $+150^\circ C$ all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|--------------------------------------------------------|----------------------------------------------------------------------|-----------------|--------------|------|------|---------|----------------------------------------|
| | | | Min. | Typ. | Max. | | |
| 100% D.C. charge pump | | | | | | | |
| 5.1.42 | Charge pump frequency ¹⁾ | f_{CP} | – | 21 | – | MHz | – |
| Motor bridge reverse polarity protection output | | | | | | | |
| 5.1.43 | High level output voltage RPP vs. VS | V_{RPP1} | – | 11 | 15 | V | $I_{Load}=0\mu A$ |
| 5.1.44 | High level output voltage RPP vs. VS | V_{RPP2} | – | 11 | 12.5 | V | $I_{Load}\geq-30\mu A$ |
| 5.1.45 | D.C. output current at RPP | I_{RPP1} | – | -110 | -150 | μA | $V_{RPP}\geq 10V$; Lowside on |
| 5.1.46 | Rise time ¹⁾ | $t_{RPPrise}$ | – | 1 | 2 | ms | $C_{LOAD}=10nF$ |
| 5.1.47 | Rise time ¹⁾ | $t_{RPPrise}$ | – | 10 | 20 | μs | $C_{LOAD}=100pF$ |
| ENA and Low quiescent current mode | | | | | | | |
| 5.1.48 | ENA propagation time to output stages switched off | t_{PENA_H-L} | – | 2.0 | 3.0 | μs | – |
| 5.1.49 | Low time of ENA signal without clearing error register | t_{RST0} | – | – | 1.2 | μs | – |
| 5.1.50 | High time of ENA signal after ENA rising edge for error logic active | t_{RST1} | 4 | 5.75 | 7 | μs | – |
| 5.1.51 | go to sleep time | t_{sleep} | 310 | 415 | 540 | μs | – |
| 5.1.52 | wake up time | t_{wake} | – | 50 | 100 | μs | $C_{REG}=2.2\mu F$; $C_{BS}=330nF$ |

1) Not subject to production test, specified by design.

2) V_{diode} is the bulk diode of the external low side MOSFET

3) normally no error flag; Error flag might be triggered by under voltage VREG caused by very high load current

5.2 Protection and Diagnostic Functions

5.2.1 Short Circuit Protection

The TLE7182EM provides a short circuit protection for the external MOSFETs by monitoring the drain-source voltage of the external MOSFETs.

This monitoring of the short circuit detection for a certain external MOSFET is active as soon as the corresponding driver output stage is set to “on” and the dead time and the blanking time are expired.

The blanking time starts when the dead time has expired and assures that the switch on process of the MOSFET is not taken into account. It is recommended to keep the switching times of the MOSFETs below the blanking time.

The short circuit detection level is adjustable in an analog way by the voltage setting at the SCDL pin. There is a 1:1 translation between the voltage applied to the SCDL pin and the drain-source voltage limit. E.g. to trigger the SCD circuit at 1 V drain-source voltage, the SCDL pin must be set to 1 V. The drain-source voltage limit can be chosen between 0.2 ... 2 V.

If after the expiration of the blanking time the drain source voltage of the observed MOSFET is still higher than the SCDL level, the SCD filter time t_{SCP} starts to run. A capacitor is charged with a current. If the capacitor voltage reaches a specific level (filter time t_{SCP}), the error signal is set and the IC goes into SCDL Error Mode. If the SCD condition is removed before the SC is detected, the capacitor is discharged with the same current. The discharging of the capacitor happens as well when the MOSFET is switched off. It has to be considered that the high side and the low side output of one phase are working with the same capacitor.

The Short Circuit protection of the TLE7182EM will be deactivated, if 5V is applied at pin SCDL.

5.2.2 SCDL Pin Open Detection

An integrated structure at the SCDL pin assures that in case of an open pin the SCDL voltage is pulled to a medium voltage level. The external MOSFETs are actively switched off and an ERR flag is set. This error is self-clearing.

5.2.3 Vs and VDH Over Voltage Warning

The TLE7182EM has an integrated over voltage warning to minimize risk of destruction of the IC at high supply voltages caused by violation of the maximum ratings. For the over voltage warning the voltage is observed at the pin VS and VDH. If the voltage level has reached, the fixed over voltage threshold V_{OVW} for the filter time t_{OV} , a warning at ERR pin is set and TLE7182EM will go in normal operation with warning.

The over voltage warning is self clearing. If the voltage at pin VS and VDH returns into the specified voltage range, the Error register will be cleared and TLE7182EM returns to normal operation mode.

It is the decision of the user, if and how to react on the over voltage warning.

5.2.4 VS Under Voltage Shutdown

The TLE7182EM has an integrated VS Under Voltage Shutdown, to assure that the behavior of the complete IC is predictable in all supply voltage ranges. As soon as the under voltage threshold V_{UVVR} is reached for a specified filter time the TLE7182EM is in VS_UVLO error mode. The error signal will be set and output stages, voltage regulator and charge pump will be switched off so the IC will go into sleep mode. An enable is necessary to restart the TLE7182EM.

5.2.5 VREG Under Voltage Warning

The TLE7182EM has an integrated under voltage warning detection at VREG. If the supply voltage at VREG reaches the VREG under voltage threshold V_{UVVR} , a warning at ERR pin is set and the TLE7182EM will go into VREG error mode. In case of VREG error mode all output stages will actively switched off to prevent low gate source voltages at the power MOSFETs causing high RDSon. If supply voltage at the VREG pin recovers; the error flag will be cleared and the TLE7182EM will return in normal operation mode.

5.2.6 Over Temperature Warning

The TLE7182EM provides an integrated digital over temperature warning to minimize risk of destruction of the IC at high temperature. The temperature will be detected by a embedded sensor. During over temperature warning the ERR signal is set and the TLE7182EM is in normal operation mode with warning.

The over temperature warning is self clearing. So if temperature is below $T_{j(PW)} - dT_{j(OW)}$, the warning will be cleared and TLE7182EM returns to normal operation mode.

It is the decision of the user to react on the over temperature warning.

5.2.7 Over Current Warning

The TLE7182EM offers an integrated over current detection. The output signal of the current sense OpAmp will be monitored. If the output signal reaches the specified voltage threshold V_{OCTH} for a certain time, over current will be detected. After the comparator the filter time t_{OC} is implemented to avoid false triggering caused by overswing of the current sense signal. The ERR pin will be set to low and the TLE7182EM will go into normal operation mode with warning.

The error signal disappears as soon as the current decreases below the over current threshold V_{OCTH} . The error signal disappears as well when the current commutates from the low side MOSFET to the associated high side MOSFET and is no longer flowing over the shunt resistor.

It is the decision of the user to react on the over current signal by modifying input patterns.

5.2.8 Passive Gxx Clamping

If VS Under Voltage shutdown is detected or the device is in Sleep Mode, a passive clamping is active as long as the voltage at VS or VDH is higher than 3V. Even below 3V it is assured that the MOSFET driver stage will not switch on the MOSFET actively.

The passive clamping means that the BHx and the VREG pin are pulled to GND with specified pull down resistors. Together with the intrinsic diode of the push stage of the output stages which connect the gate output to BHx respectively VREG, this assures that the gate of the external MOSFETs are not floating undefined.

5.2.9 $\overline{\text{ERR}}$ Pin

The TLE7182EM has a status pin to provide diagnostic feedback to the μC . The logical output of this pin is a push pull output stage with an integrated pull-down resistor to GND (see [Figure 4](#)).

Reset of error registers and Disable

The TLE7182EM can be reset by the enable pin ENA. If the ENA pin is pulled to low for a specified minimum time, the error registers are cleared. ERR output is still set to low. After the next rising edge at ENA pin ERR pin will be set to high and no error condition is applied.

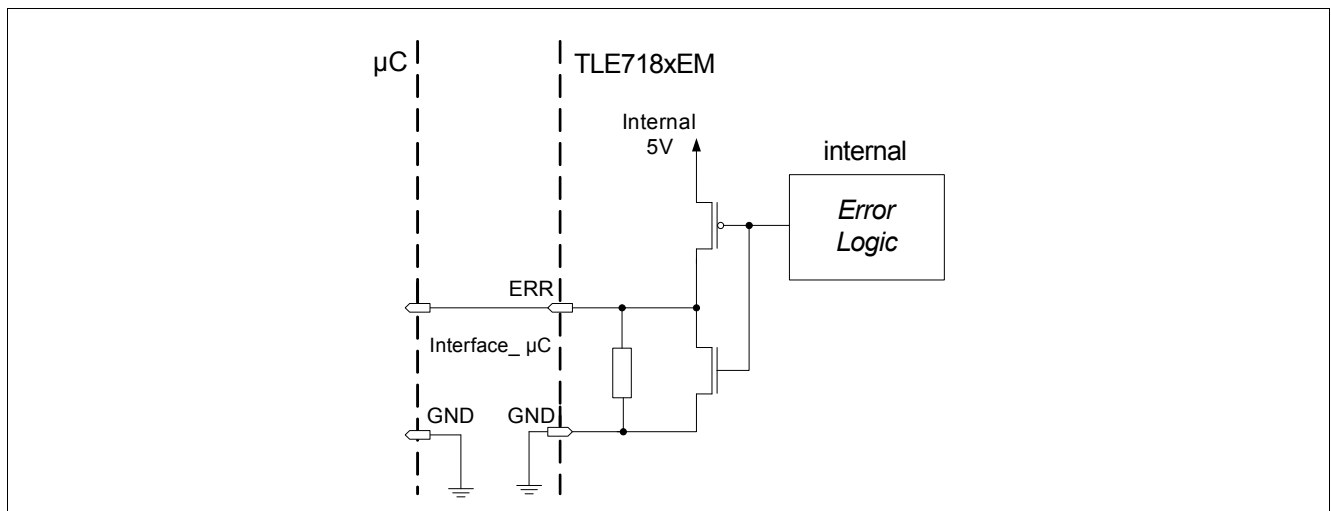


Figure 4 Structure of ERR output

Table 5 Overview of error condition

| ERR | Driver conditions | Driver action | Restart |
|------|------------------------------------|----------------------------------------|---------------------------------------------------------|
| High | no errors | Fully functional | – |
| Low | Over temperature | Warning only | Self clearing |
| Low | Over voltage VS/VDH | Warning only | Self clearing |
| Low | Over current OPAMP | Warning only | Self clearing |
| Low | Under voltage error VREG | All MOSFETs actively switched off | Self clearing |
| Low | Under voltage shutdown based on VS | MOSFET, charge pump, Vreg switched off | Self clearing restart when enable high ¹⁾ |
| Low | SCDL open pin | All MOSFETs actively switched off | Self clearing |
| Low | Short circuit detection | All MOSFETs actively switched off | Reset at ENA needed |
| Low | Go to sleep mode | All MOSFETs actively switched off | immediate restart when ENA goes high |
| Low | Wake up mode | start up | – |

1) When SC detected, reset with ENA necessary

Table 6 Prioritization of Errors

| Priority | Errors and Warnings |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | Under voltage lockout at Vs (VS_UVLO) |
| 1 | Short circuit detection error (SCD) SCDL pin open warning (SCDLPOD) |
| 2 | Under voltage detection VREG (UV_VREG) Over voltage detection warning (OVD) Over temperature warning (OTD) Over current warning (OCD) |

5.2.10 Electrical Characteristics

Electrical Characteristics - Protection and diagnostic functions

$V_S = 7.0$ to $34V$, $T_j = -40$ to $+150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|-------------------------------------------|------------------------------------------------------------------------------------------------------------------|----------------|--------------|------|------|------------|--------------------------------------|
| | | | Min. | Typ. | Max. | | |
| Short circuit protection | | | | | | | |
| 5.2.1 | Short circuit protection detection level input range | V_{SCDL} | 0.2 | – | 2.0 | V | programmed by SCDL pin |
| 5.2.2 | Short circuit protection detection accuracy | A_{SCP1} | -50 | – | +50 | % | $0.2V \leq V_{SCDL} \leq 0.3V$ |
| 5.2.3 | Short circuit protection detection accuracy | A_{SCP2} | -30 | – | +30 | % | $0.3V \leq V_{SCDL} \leq 1.2V$ |
| 5.2.4 | Short circuit protection detection accuracy | A_{SCP3} | -10 | – | +10 | % | $1.2V \leq V_{SCDL} \leq 2.0V$ |
| 5.2.5 | Filter time of short circuit protection | $t_{SCP(off)}$ | 2.5 | 3.5 | 4.5 | μs | – |
| 5.2.6 | Filter time and blanking time of short circuit protection | t_{SCPBT} | 4 | 6 | 8 | μs | – |
| 5.2.7 | Internal pull-up resistor SCDL to 3V | R_{SCDL} | 180 | 300 | 475 | k Ω | – |
| 5.2.8 | SCDL open pin detection level | V_{SCPOP} | 2.1 | – | 3.2 | V | – |
| 5.2.9 | Filter time of SCDL open pin detection | t_{SCPOP} | 1.5 | 2.5 | 3.5 | μs | – |
| 5.2.10 | SCDL open pin detection level hysteresis ¹⁾ | V_{SCOPH} | – | 0.3 | – | V | – |
| 5.2.11 | Threshold voltage for deactivation of: - SC detection - dead-time generation - shoot-through protection | V_{SCPDIS} | 4.5 | – | – | V | – |
| 5.2.12 | Filter time of SCD deactivation | t_{SCPDIS} | 1.0 | 2.0 | 3.1 | μs | – |
| Over- and under voltage monitoring | | | | | | | |
| 5.2.13 | Over voltage warning at V_S and/or V_{DH} | V_{OVW} | 34.5 | 36.5 | 38.5 | V | V_{VS} and/or V_{VDH} increasing |
| 5.2.14 | Over voltage warning hysteresis for V_S and/or V_{DH} | V_{OVWhys} | 2.1 | 3.1 | 4.1 | V | – |
| 5.2.15 | Over voltage warning filter time for V_S and/or V_{DH} | t_{OV} | 13 | 19 | 25 | μs | – |
| 5.2.16 | Under voltage shutdown at V_S | V_{UVVR} | 4.5 | 5.0 | 5.5 | V | V_{VS} decreasing |
| 5.2.17 | Under voltage shutdown filter time for V_S ¹⁾ | t_{UVLO} | – | 20 | – | μs | – |
| 5.2.18 | Under voltage warning at VREG | V_{UVVR} | 5.5 | 6.0 | 6.5 | V | V_{VS} decreasing |
| 5.2.19 | Under voltage diagnosis filter time for VREG | t_{UVVR} | 10 | – | 30 | μs | – |
| 5.2.20 | Under voltage hysteresis at VREG | V_{UVRhys} | – | 0.5 | – | V | – |

Electrical Characteristics - Protection and diagnostic functions (cont'd)

$V_S = 7.0$ to $34V$, $T_j = -40$ to $+150^\circ C$, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|-------------------------------|-----------------------------------------|--------------|--------------|------|------|------------|------------------|
| | | | Min. | Typ. | Max. | | |
| Temperature monitoring | | | | | | | |
| 5.2.21 | Over temperature warning | $T_{j(PW)}$ | 160 | 170 | 180 | $^\circ C$ | – |
| 5.2.22 | Hysteresis for over temperature warning | $dT_{j(OW)}$ | 10 | – | 20 | $^\circ C$ | – |
| Over current detection | | | | | | | |
| 5.2.23 | Over current detection level | V_{OCTH} | 4.5 | – | 4.99 | V | – |
| 5.2.24 | Filter time for over current detection | t_{OC} | 2.3 | – | 4.3 | μs | – |
| ERR pin²⁾ | | | | | | | |
| 5.2.25 | ERR output voltage | V_{ERR} | 4.6 | – | – | V | $V_{VS}=7V$; |
| 5.2.26 | Rise time ERR (20 - 80% of internal 5V) | $t_{f(ERR)}$ | – | – | 3 | μs | $C_{LOAD}=1nF$; |
| 5.2.27 | Internal pull-down resistor ERR to GND | $R_{f(ERR)}$ | 60 | 100 | 170 | $k\Omega$ | – |

1) Not subject to production test, specified by design.

2) ERR pin and Reset & Enable functional between $V_{VS}=6 \dots 7V$, but characteristics might be out of specified range

5.3 Shunt Signal Conditioning

The TLE7182EM incorporates a fast and precise operational amplifier for conditioning and amplification of the current sense shunt signal. The gain of the OpAmp is adjustable by external resistors within a range higher than 5. The usage of higher gains in the application might be limited by required settling time and band width.

It is recommended to apply a small offset to the OpAmp, to avoid operation in the lower rail at low currents.

The output of the OpAmp ISO is not short-circuit proof.

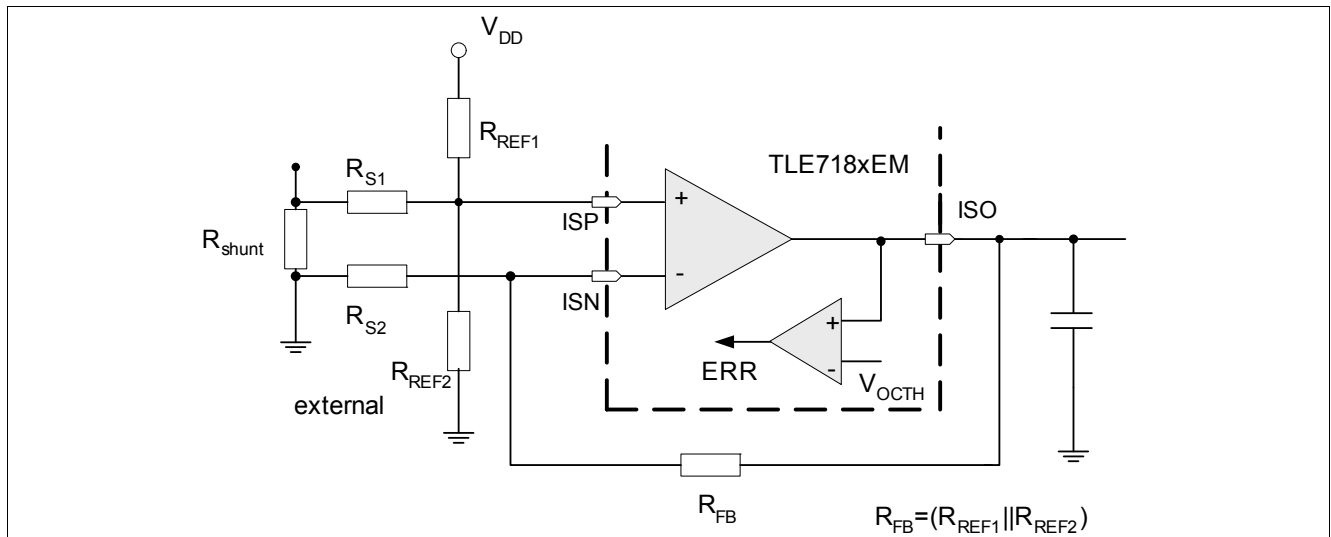


Figure 5 Shunt Signal Conditioning Block Diagram and Over Current Limitation

Over current warning see [Chapter 5.2.7](#).

5.3.1 Electrical Characteristics

Electrical Characteristics - Current sense signal conditioning

$V_S = 7.0$ to $36V$, $T_j = -40$ to $+150^\circ C$, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|-------|--------------------------------------------------------------------------|--------------|--------------|------|------|----------|---------------------------------------------------|
| | | | Min. | Typ. | Max. | | |
| 5.3.1 | Series resistors | R_S | 100 | 500 | 1000 | Ω | – |
| 5.3.2 | Feedback resistor Limited by the output voltage dynamic range | R_{fb} | 2000 | 7500 | – | Ω | – |
| 5.3.3 | Resistor ratio (gain ratio) | R_{fb}/R_S | 5 | – | – | – | – |
| 5.3.4 | Steady state differential input voltage range across VIN | $V_{IN(ss)}$ | -400 | – | 400 | mV | – |
| 5.3.5 | Input differential voltage (ISP - ISN) | V_{IDR} | -800 | – | 800 | mV | – |
| 5.3.6 | Input voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND) | V_{LL} | -800 | – | 2000 | mV | – |
| 5.3.7 | Input offset voltage of the I-DC link OpAmp, including temperature drift | V_{IO} | – | – | +/-2 | mV | $R_S=500\Omega$; $V_{CM}=0V$; $V_{ISO}=1.65V$; |
| 5.3.8 | Input bias current (ISN,ISP to GND) | I_{IB} | -300 | – | – | μA | $V_{CM}=0V$; $V_{ISO}=open$ |
| 5.3.9 | Low level output voltage of ISO | V_{OL} | -0.1 | – | 0.2 | V | $I_{OH}=3mA$ |

Electrical Characteristics - Current sense signal conditioning (cont'd)

$V_S = 7.0$ to $36V$, $T_j = -40$ to $+150^\circ C$, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Conditions |
|--------|------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------|----------------|------|------------|---------------------------------------------------------------------------------------------------------------|
| | | | Min. | Typ. | Max. | | |
| 5.3.10 | High level output voltage of ISO | V_{OH} | 4.75 | – | 5.2 | V | $I_{OH} = -3mA$ |
| 5.3.11 | Output short circuit current | I_{SCOP} | 5 | – | – | mA | – |
| 5.3.12 | Differential input resistance ¹⁾ | R_I | 100 | – | – | k Ω | – |
| 5.3.13 | Common mode input capacitance ¹⁾ | C_{CM} | – | – | 10 | pF | 10kHz |
| 5.3.14 | Common mode rejection ratio at DC CMRR = $20 \cdot \log((V_{out_diff}/V_{in_diff}) \cdot (V_{in_CM}/V_{out_CM}))$ | C_{MRR} | 80 | 100 | – | dB | – |
| 5.3.15 | Common mode suppression ²⁾ with CMS = $20 \cdot \log(V_{out_CM}/V_{in_CM})$ Freq = 100kHz Freq = 1MHz Freq = 10MHz | C_{MS} | – | 62 43 23 | – | dB | $V_{IN} = 360mV \cdot \sin(2 \cdot \pi \cdot freq \cdot t)$; $R_s = 500\Omega$; $R_{fb} = 7500\Omega$ |
| 5.3.16 | Slew rate | $d_{V/dt}$ | – | 10 | – | V/ μs | Gain ≥ 5 ; $R_L = 1.0k\Omega$; $C_L = 500pF$ |
| 5.3.17 | Large signal open loop voltage gain (DC) | A_{OL} | 80 | 100 | – | dB | – |
| 5.3.18 | Unity gain bandwidth ¹⁾ | G_{BW} | 10 | 20 | – | MHz | $R_L = 1k\Omega$; $C_L = 100pF$ |
| 5.3.19 | Phase margin ¹⁾ | F_M | – | 50 | – | ° | Gain ≥ 5 ; $R_L = 1k\Omega$; $C_L = 100pF$ |
| 5.3.20 | Gain margin ¹⁾ | A_M | – | 12 | – | dB | $R_L = 1k\Omega$; $C_L = 100pF$ |
| 5.3.21 | Bandwidth | B_{WG} | 0.7 | 1.3 | – | MHz | Gain = 15; $R_L = 1k\Omega$; $C_L = 500pF$; $R_s = 500\Omega$ |
| 5.3.22 | Output settle time to 98% | t_{set1} | – | 1 | 1.8 | μs | Gain = 15; $R_L = 1k\Omega$; $C_L = 500pF$; $0.3 < V_{ISO} < 4.8V$; $R_s = 500\Omega$ |
| 5.3.23 | Output settle time to 98% ¹⁾ | t_{set2} | – | 4.6 | – | μs | Gain = 75; $R_L = 1k\Omega$; $C_L = 500pF$; $0.3 < V_{ISO} < 4.8V$; $R_s = 500\Omega$ |

1) Not subjected to production test; specified by design

2) Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This is the description how the IC is used in its environment...

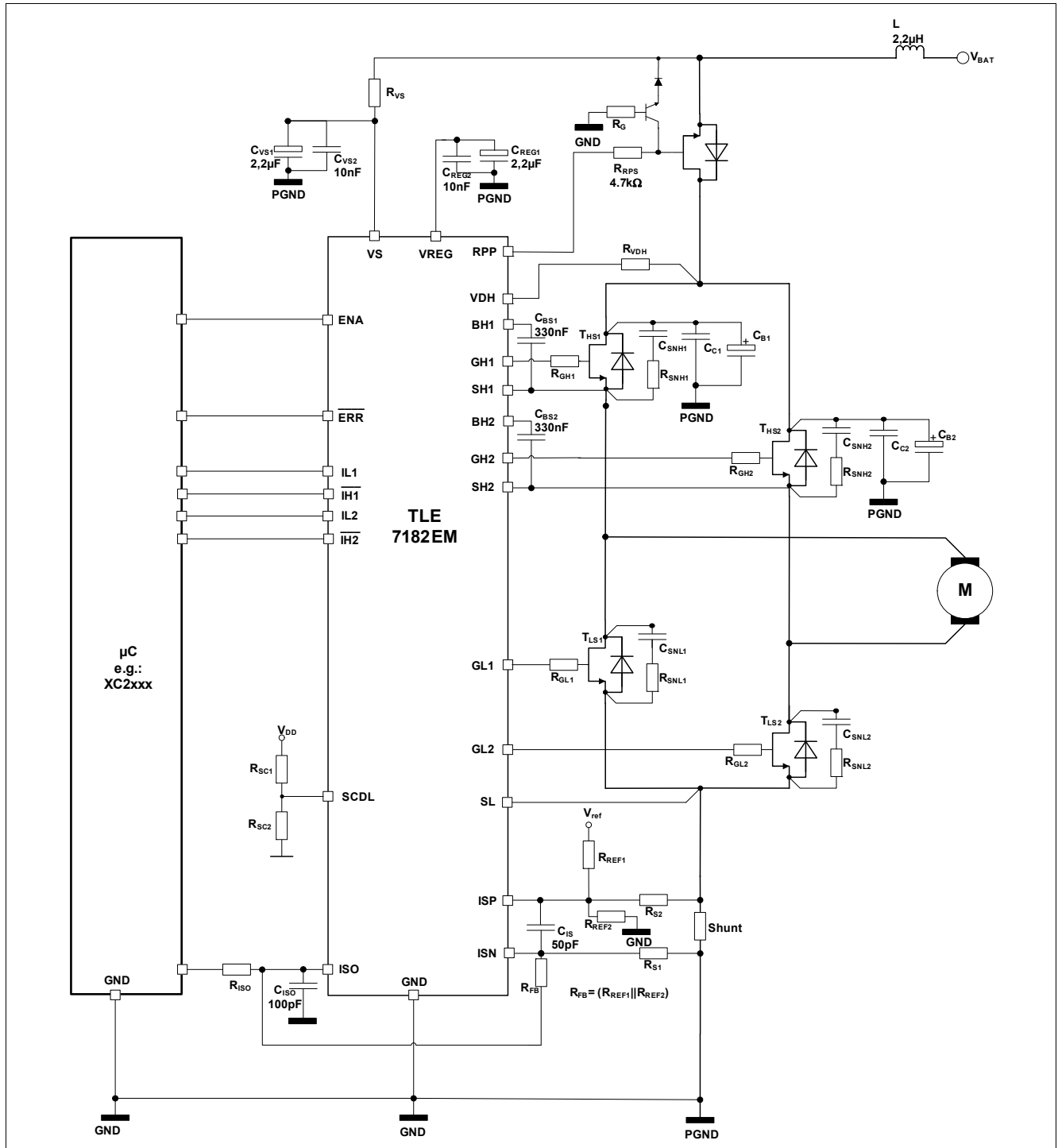


Figure 6 Application Diagram 1: DC-Brush motor controlled by TLE7182EM

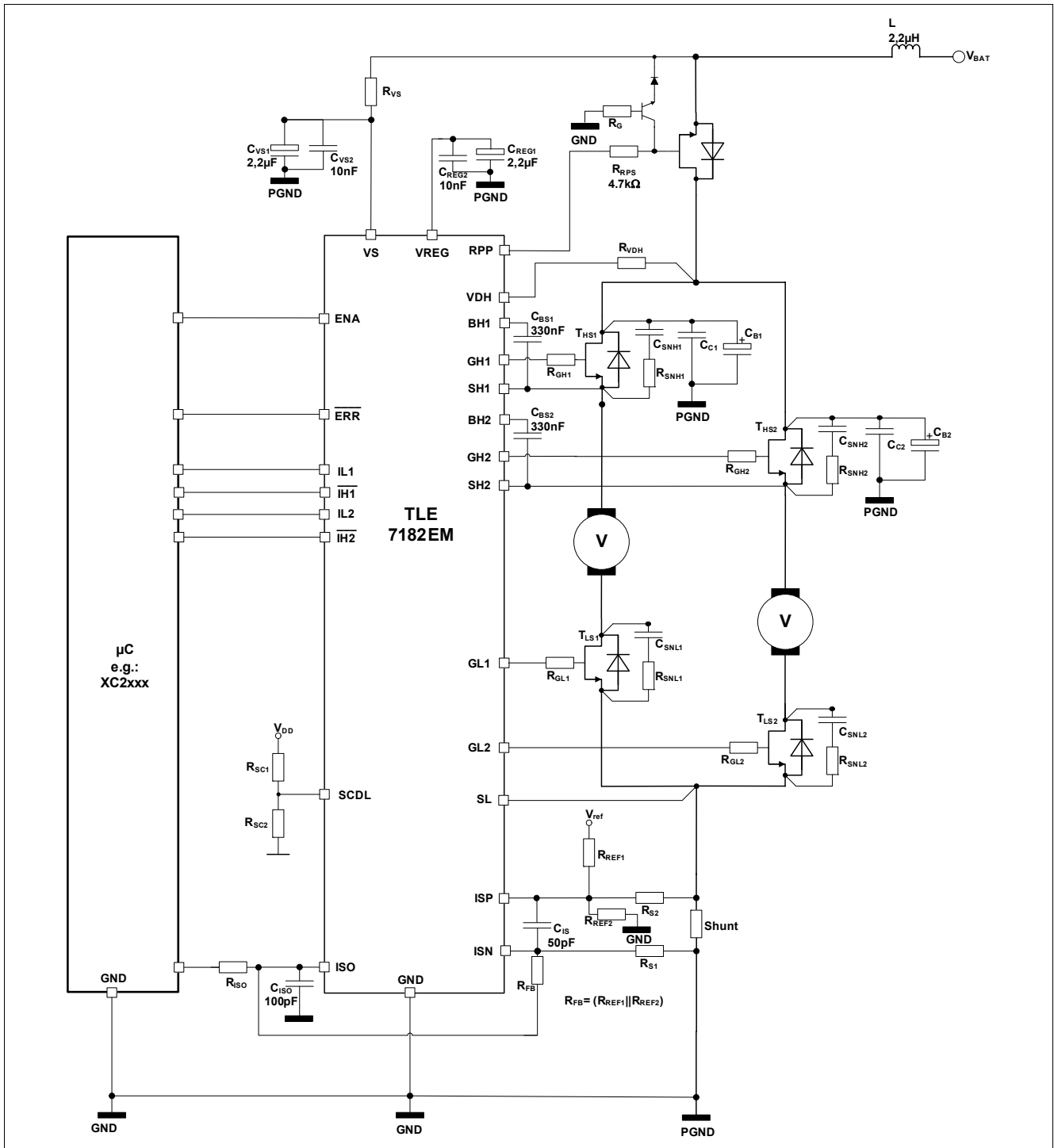


Figure 7 Application Diagram 2: 2 inductive loads driven by TLE7182EM

Note: This are very simplified examples of an application circuit. The function must be verified in the real application.

6.1 Layout Guide Lines

Please refer also to the simplified application example.

- Two separated bulk capacitors C_B should be used - one per half bridge
- Two separated ceramic capacitors C_C should be used - one per half bridge
- Each of the two bulk capacitors C_B and each of the two ceramic capacitors C_C should be assigned to one of the half bridges and should be placed very close to it
- The components within one half bridge should be placed close to each other: high side MOSFET, low side MOSFET, bulk capacitor C_B and ceramic capacitor C_C (C_B and C_C are in parallel) and the shunt resistor form a loop that should be as small and tight as possible. The traces should be short and wide
- The connection between the source of the high side MOSFET and the drain of the low side MOSFET should be as low inductive and as low resistive as possible.
- VDH is the sense pin used for short circuit detection; VDH should be routed (via Rvdh) to the common point of the drains of the high side MOSFETs to sense the voltage present on drain high side
- SL is the sense pin used for short circuit detection; SL should be routed to the common point of the source of the low side MOSFETs to sense the voltage present on source low side
- Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors)
- if available the exposed pad on the backside of the package should be connected to GND

6.2 Further Application Information

- For further information you may contact <http://www.infineon.com/>

8 Revision History

| Revision | Date | Changes |
|----------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.1 | 2010-09-30 | Datasheet Max rating of current at RPP pin increased |
| 1.0 | 2010-09-29 | Datasheet Thermal resistance of package adjusted Output rise time adjusted Pull up and pull down resistor values adapted Dead time values centered Go to sleep time modified Filter time of short circuit detection adjusted SCDL pin open detection description improved Overview of error condition table improved Filter time and blanking time of short circuit detection adjusted SCDL open pin detection level added Filter time of SCDL open pin detection adjusted Over voltage warning at Vs and/or VDH centered Over voltage warning hysteresis for Vs and/or VDH centered Over voltage warning filter time for Vs and/or VDH centered ERR output voltage added OpAmp bandwidth adjusted |
| 0.8 | 2010-08-31 | Preliminary Datasheet |
| 0.7 | 2009-11-19 | Target data sheet |
| 0.6 | 2008-30-10 | Target data sheet |

Edition 2010-09-30

**Published by
Infineon Technologies AG
81726 Munich, Germany**

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